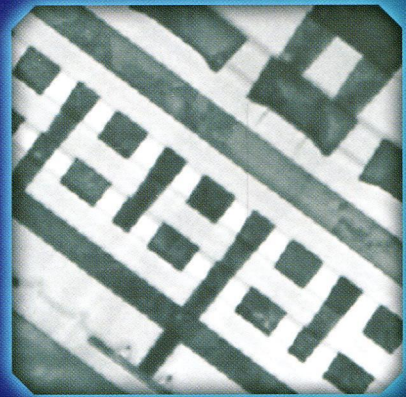


Editors

Mikhail R. Baklanov, Paul S. Ho  
and Ehrenfried Zschech

# Advanced Interconnects for ULSI Technology



 WILEY

# **Advanced Interconnects for ULSI Technology**

Edited by

Mikhail R. Baklanov, Paul S. Ho and Ehrenfried Zschech



A John Wiley & Sons, Ltd., Publication

This edition first published 2012  
© 2012 John Wiley & Sons, Ltd

*Registered Office*

John Wiley & Sons, Ltd, The Atrium, Southern Gate, Chichester, West Sussex, PO19 8SQ, United Kingdom

For details of our global editorial offices, for customer services and for information about how to apply for permission to reuse the copyright material in this book please see our website at [www.wiley.com](http://www.wiley.com).

The right of the author to be identified as the author of this work has been asserted in accordance with the Copyright, Designs and Patents Act 1988.

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, except as permitted by the UK Copyright, Designs and Patents Act 1988, without the prior permission of the publisher.

Wiley also publishes its books in a variety of electronic formats. Some content that appears in print may not be available in electronic books.

Designations used by companies to distinguish their products are often claimed as trademarks. All brand names and product names used in this book are trade names, service marks, trademarks or registered trademarks of their respective owners. The publisher is not associated with any product or vendor mentioned in this book. This publication is designed to provide accurate and authoritative information in regard to the subject matter covered. It is sold on the understanding that the publisher is not engaged in rendering professional services. If professional advice or other expert assistance is required, the services of a competent professional should be sought.

The publisher and the author make no representations or warranties with respect to the accuracy or completeness of the contents of this work and specifically disclaim all warranties, including without limitation any implied warranties of fitness for a particular purpose. This work is sold with the understanding that the publisher is not engaged in rendering professional services. The advice and strategies contained herein may not be suitable for every situation. In view of ongoing research, equipment modifications, changes in governmental regulations, and the constant flow of information relating to the use of experimental reagents, equipment, and devices, the reader is urged to review and evaluate the information provided in the package insert or instructions for each chemical, piece of equipment, reagent, or device for, among other things, any changes in the instructions or indication of usage and for added warnings and precautions. The fact that an organization or Website is referred to in this work as a citation and/or a potential source of further information does not mean that the author or the publisher endorses the information the organization or Website may provide or recommendations it may make. Further, readers should be aware that Internet Websites listed in this work may have changed or disappeared between when this work was written and when it is read. No warranty may be created or extended by any promotional statements for this work. Neither the publisher nor the author shall be liable for any damages arising herefrom.

*Library of Congress Cataloging-in-Publication Data*

Advanced interconnects for ULSI technology / [edited by] Mikhail R. Baklanov, Paul S. Ho, Ehrenfried Zschech.  
p. cm.

Includes bibliographical references and index.

ISBN 978-0-470-66254-0 (hardback)

I. Interconnects (Integrated circuit technology). 2. Integrated circuits—Ultra large scale integration.

I. Baklanov, Mikhail. II. Ho, P. S. III. Zschech, Ehrenfried.

TK7874.53.A39 2012

621.39'5—dc23

2011038787

A catalogue record for this book is available from the British Library.

Print ISBN: 9780470662540

Set in 10/12pt Times by SPi Publisher Services, Pondicherry, India  
Printed and bound in Singapore by Markono Print Media Pte Ltd

# Contents

<i>About the Editors</i>	<b>xiii</b>
<i>List of Contributors</i>	<b>xv</b>
<i>Preface</i>	<b>xix</b>
<i>Abbreviations</i>	<b>xxiii</b>
<b>Section I Low-<i>k</i> Materials</b>	<b>1</b>
<b>1 Low-<i>k</i> Materials: Recent Advances</b>	<b>3</b>
<i>Geraud Dubois and Willi Volksen</i>	
1.1 Introduction	3
1.2 Integration Challenges	5
1.2.1 Process-Induced Damage	6
1.2.2 Mechanical Properties	9
1.3 Processing Approaches to Existing Integration Issues	10
1.3.1 Post-deposition Treatments	11
1.3.2 Prevention or Repair of Plasma-Induced Processing Damage	14
1.3.3 Multilayer Structures	15
1.4 Material Advances to Overcome Current Limitations	16
1.4.1 Silica Zeolites	16
1.4.2 Hybrid Organic–Inorganic: Oxycarbosilanes	19
1.5 Conclusion	22
References	23
<b>2 Ultra-Low-<i>k</i> by CVD: Deposition and Curing</b>	<b>35</b>
<i>Vincent Jousseume, Aziz Zenasni, Olivier Gourhant, Laurent Favennec and Mikhail R. Baklanov</i>	
2.1 Introduction	35
2.2 Porogen Approach by PECVD	37
2.2.1 Precursors and Deposition Conditions	37
2.2.2 Mystery Still Unsolved: From Porogens to Pores	41
2.3 UV Curing	42
2.3.1 General Overview of Curing	42
2.3.2 UV Curing Mechanisms	43
2.4 Impact of Curing on Structure and Physical Properties: Benefits of UV Curing	49
2.4.1 Porosity	49

2.4.2	Chemical Structure and Mechanical Properties	50
2.4.3	Electrical Properties	56
2.5	Limit/Issues with the Porogen Approach	57
2.5.1	Porosity Creation Limit	58
2.5.2	Porogen Residues	59
2.6	Future of CVD Low- <i>k</i>	62
2.6.1	New Matrix Precursor	62
2.6.2	Other Deposition Strategies	64
2.6.3	New Deposition Techniques	66
2.7	Material Engineering: Adaptation to Integration Schemes	68
2.8	Conclusion	70
	References	71
<b>3</b>	<b>Plasma Processing of Low-<i>k</i> Dielectrics</b>	<b>79</b>
	<i>Hualiang Shi, Denis Shamiryam, Jean-François de Marneffe, Huai Huang, Paul S. Ho and Mikhail R. Baklanov</i>	
3.1	Introduction	79
3.2	Materials and Equipment	80
3.3	Process Results Characterization	82
3.4	Interaction of Low- <i>k</i> Dielectrics with Plasma	85
3.4.1	Low- <i>k</i> Etch Chemistries	85
3.4.2	Patterning Strategies and Masking Materials	87
3.4.3	Etch Mechanisms	88
3.5	Mechanisms of Plasma Damage	92
3.5.1	Gap Structure Studies	93
3.5.2	Effect of Radical Density	95
3.5.3	Effect of Ion Energy	96
3.5.4	Effect of Photon Energy and Intensity	99
3.5.5	Plasma Damage by Oxidative Radicals	103
3.5.6	Hydrogen-Based Plasma	105
3.5.7	Minimization of Plasma Damage	108
3.6	Dielectric Recovery	112
3.6.1	CH <sub>4</sub> Beam Treatment	112
3.6.2	Dielectric Recovery by Silylation	113
3.6.3	UV Radiation	119
3.7	Conclusions	121
	References	122
<b>4</b>	<b>Wet Clean Applications in Porous Low-<i>k</i> Patterning Processes</b>	<b>129</b>
	<i>Quoc Toan Le, Guy Vereecke, Herbert Struyf, Els Kesters and Mikhail R. Baklanov</i>	
4.1	Introduction	129
4.2	Silica and Porous Hybrid Dielectric Materials	130
4.3	Impact of Plasma and Subsequent Wet Clean Processes on the Stability of Porous Low- <i>k</i> Dielectrics	134

4.3.1	Stability in Pure Chemical Solutions	134
4.3.2	Stability in Commercial Chemistries	135
4.3.3	Hydrophobicity of Hybrid Low- <i>k</i> Materials	138
4.4	Removal of Post-Etch Residues and Copper Surface Cleaning	141
4.5	Plasma Modification and Removal of Post-Etch 193 nm Photoresist	146
4.5.1	Modification of 193 nm Photoresist by Plasma Etch	146
4.5.2	Wet Removal of 193 nm Photoresist	153
	Acknowledgments	166
	References	166
<b>Section II Conductive Layers and Barriers</b>		<b>173</b>
<b>5</b>	<b>Copper Electroplating for On-Chip Metallization</b>	<b>175</b>
	<i>Valery M. Dubin</i>	
5.1	Introduction	175
5.2	Copper Electroplating Techniques	176
5.3	Copper Electroplating Superfill	177
5.3.1	The Role of Accelerator	177
5.3.2	The Role of Suppressor	178
5.3.3	The Role of Leveler	180
5.4	Alternative Cu Plating Methods	182
5.4.1	Electroless Plating	182
5.4.2	Direct Plating	182
5.5	Electroplated Cu Properties	184
5.5.1	Resistivity	184
5.5.2	Impurities	184
5.5.3	Electromigration	185
5.6	Conclusions	186
	References	187
<b>6</b>	<b>Diffusion Barriers</b>	<b>193</b>
	<i>Michael Hecker and René Hübner</i>	
6.1	Introduction	193
6.1.1	Cu Metallization, Barrier Requirements and Materials	193
6.1.2	Barrier Deposition Techniques	195
6.1.3	Characterization of Barrier Performance	196
6.2	Metal-Based Barriers as Liners for Cu Seed Deposition	198
6.2.1	Ta-Based Barriers	198
6.2.2	W-Based Barriers	209
6.2.3	Ti-Based Barriers	210
6.2.4	Further Systems	211
6.3	Advanced Barrier Approaches	212
6.3.1	Barriers for Direct Cu Plating	212
6.3.2	Metal Capping Layers	214
6.3.3	Self-Forming Diffusion Barriers	216

6.3.4	Self-Assembled Molecular Nanolayers and Polymer-Based Barriers	218
6.4	Conclusions	221
	References	221
<b>Section III Integration and Reliability</b>		<b>235</b>
<b>7</b>	<b>Process Integration of Interconnects</b>	<b>237</b>
	<i>Sridhar Balakrishnan, Ruth Brain and Larry Zhao</i>	
7.1	Introduction	237
7.2	On-Die Interconnects in the Submicrometer Era	237
7.3	On-Die Interconnects at Sub-100 nm Nodes	240
7.4	Integration of Low- $k$ Dielectrics in Sub-65 nm Nodes	241
7.4.1	Degradation of Dielectric Constant during Integration	243
7.4.2	Integration Issues in ELK Dielectrics Due to Degraded Mechanical Properties	246
7.5	Patterning Integration at Sub-65 nm Nodes	248
7.5.1	Patterning Challenges	249
7.6	Integration of Conductors in Sub-65 nm Nodes	252
7.6.1	Narrow Line Copper Resistivity	253
7.6.2	Integrating Novel Barrier/Liner Materials and Deposition Techniques for Cu Interconnects	254
7.6.3	Self-Forming Barriers and Their Integration	256
7.6.4	Integration to Enable Reliable Copper Interconnects	257
7.7	Novel Air-Gap Interconnects	258
7.7.1	Unlanded Via Integration with Air-Gap Interconnects	258
7.7.2	Air-Gap Formation Using Nonconformal Dielectric Deposition	259
7.7.3	Air-Gap Formation Using a Sacrificial Material	260
	References	261
<b>8</b>	<b>Chemical Mechanical Planarization for Cu-Low-<math>k</math> Integration</b>	<b>267</b>
	<i>Gautam Banerjee</i>	
8.1	Introduction	267
8.2	Back to Basics	268
8.3	Mechanism of the CMP Process	268
8.4	CMP Consumables	271
8.4.1	Slurry	271
8.4.2	Pad	273
8.4.3	Pad Conditioner	274
8.5	CMP Interactions	276
8.6	Post-CMP Cleaning	281
8.6.1	Other Defects	286
8.6.2	Surface Finish	286
8.6.3	E-Test	287
8.7	Future Direction	287
	References	288

<b>9</b>	<b>Scaling and Microstructure Effects on Electromigration Reliability for Cu Interconnects</b>	<b>291</b>
	<i>Chao-Kun Hu, René Hübner, Lijuan Zhang, Meike Hauschildt and Paul S. Ho</i>	
9.1	Introduction	291
9.2	Electromigration Fundamentals	293
9.2.1	EM Mass Flow	293
9.2.2	EM Lifetime and Scaling Rule	294
9.2.3	Statistical Test Method	296
9.2.4	Effect of Current Density on EM Lifetime	297
9.3	Cu Microstructure	299
9.3.1	X-ray Diffraction (XRD)	299
9.3.2	Electron Backscatter Diffraction in the Scanning Electron Microscope	301
9.3.3	Orientation Imaging Microscopy in the Transmission Electron Microscope	304
9.4	Lifetime Enhancement	306
9.4.1	Effect of a Ta Liner	306
9.4.2	Upper-Level Dummy Vias	308
9.4.3	Plasma Pre-clean and SiH <sub>4</sub> Soak	310
9.4.4	CVD and ECD Cu and the Effect of Nonmetallic Impurities	311
9.4.5	Cu Alloys	314
9.4.6	CoWP Cap Near-Bamboo and Polycrystalline Cu Lines	319
9.5	Effect of Grain Size on EM Lifetime and Statistics	321
9.6	Massive-Scale Statistical Study of EM	326
9.7	Summary	329
	Acknowledgments	331
	References	331
<b>10</b>	<b>Mechanical Reliability of Low-<i>k</i> Dielectrics</b>	<b>339</b>
	<i>Kris Vanstreels, Han Li and Joost J. Vlassak</i>	
10.1	Introduction	339
10.2	Mechanical Properties of Porous Low- <i>k</i> Materials	340
10.2.1	Techniques to Measure Mechanical Properties of Thin Films	340
10.2.2	Effect of Porosity on the Stiffness of Organosilicate Glass Films	342
10.2.3	Hybrid Dielectrics Containing Organic/Inorganic Bridging Units	344
10.2.4	Effect of UV Wavelength and Porogen Content on the Hardening Process of PECVD Low- <i>k</i> Dielectrics	349
10.3	Fracture Properties of Porous Low- <i>k</i> Materials	352
10.3.1	Adhesion Measurement Methods	352
10.3.2	Fracture Toughness Measurement Techniques	354
10.3.3	Effect of Porosity and Network Structure on the Fracture Toughness of Organosilicate Glass Films	355



10.3.4	Effects of UV Cure on Fracture Properties of Carbon-Doped Oxides	357
10.3.5	Water Diffusion and Fracture Properties of Organosilicate Glass Films	359
10.4	Conclusion	361
	References	362
<b>11</b>	<b>Electrical Breakdown in Advanced Interconnect Dielectrics</b>	<b>369</b>
	<i>Ennis T. Ogawa and Oliver Auel</i>	
11.1	Introduction	369
11.1.1	Dual-Damascene Integration of Low- <i>k</i> Dielectrics	370
11.1.2	Low- <i>k</i> Types and Integrating Low- <i>k</i> Dielectrics	373
11.2	Reliability Testing	378
11.2.1	Measurement of Dielectric Degradation	378
11.2.2	Reliability Analysis	390
11.3	Lifetime Extrapolation and Models	397
11.4	Future Trends and Concerns	403
	Acknowledgments	405
	References	405
<b>Section IV</b>	<b>New Approaches</b>	<b>435</b>
<b>12</b>	<b>3D Interconnect Technology</b>	<b>437</b>
	<i>John U. Knickerbocker, Lay Wai Kong, Sven Niese, Alain Diebold and Ehrenfried Zschech</i>	
12.1	Introduction	437
12.2	Dimensional Interconnected Circuits (3DICs) for System Applications	438
	<i>John U. Knickerbocker</i>	
12.2.1	Introduction	438
12.2.2	System Needs	441
12.2.3	3D Interconnect Design and Architecture	444
12.2.4	3D Fabrication and Interconnect Technology	446
12.2.5	Trade-offs in Application Design and Product Applications	464
12.2.6	Summary	466
	Acknowledgments	467
12.3	Advanced Microscopy Techniques for 3D Interconnect Characterization	467
	<i>Lay Wai Kong, Sven Niese, Alain Diebold and Ehrenfried Zschech</i>	
12.3.1	Scanning Acoustic Microscopy	467
12.3.2	IR Microscopy	473
12.3.3	Transmission X-ray Microscopy and Tomography	474
12.3.4	Microstructure Analysis	480
12.4	Summary	486
	References	486

<b>13</b>	<b>Carbon Nanotubes for Interconnects</b>	<b>491</b>
	<i>Mizuhisa Nihei, Motonobu Sato, Akio Kawabata, Shintaro Sato and Yuji Awano</i>	
13.1	Introduction	491
13.2	Advantage of CNT Vias	492
13.3	Fabrication Processes of CNT Vias	493
13.4	Electrical Properties of CNT Vias	496
13.5	Current Reliability of CNT Vias	498
13.6	Conclusion	501
	Acknowledgments	501
	References	501
<b>14</b>	<b>Optical Interconnects</b>	<b>503</b>
	<i>Wim Bogaerts</i>	
14.1	Introduction	503
14.2	Optical Links	505
14.2.1	Waveguides	507
14.2.2	Waveguide Filters and (De)multiplexers	510
14.2.3	Transmitter: Light Source	513
14.2.4	Transmitter: Modulators	514
14.2.5	Receiver: Photodetector	517
14.2.6	Power Consumption and Heat Dissipation	517
14.2.7	Different Materials	518
14.2.8	Conclusion	519
14.3	The Case for Silicon Photonics	519
14.3.1	Waveguides and WDM Components	519
14.3.2	Modulators, Tuners and Switches	523
14.3.3	Photodetectors	526
14.3.4	Light Sources	526
14.3.5	Conclusion	527
14.4	Optical Networks on a Chip	528
14.4.1	WDM Point-to-Point Links	529
14.4.2	Bus Architecture	529
14.4.3	(Reconfigurable) Networks	530
14.5	Integration Strategies	532
14.5.1	Front-End-of-Line Integration	533
14.5.2	Backside Integration	535
14.5.3	Back-End-of-Line Integration	535
14.5.4	3D Integration	536
14.5.5	Flip-Chip Integration	537
14.5.6	Conclusion	537
14.6	Conclusion	538
	References	538

<b>15</b>	<b>Wireless Interchip Interconnects</b>	<b>543</b>
	<i>Takamaro Kikkawa</i>	
15.1	Introduction	543
15.2	Wireless Interconnect Technologies	547
15.2.1	Figure of Merit for Wireless Interconnects	547
15.2.2	Capacitively Coupled Wireless Interconnects	549
15.2.3	Inductively Coupled Wireless Interconnects	550
15.2.4	Antennas and Propagation	553
15.3	Conclusion	561
	References	561
	<b><i>Index</i></b>	<b>565</b>