IEEE DESIGN & TEST May/June 2016

IEEE

MAY/JUNE 2016

Design&Test

Robust 3-D Stacked ICs

- The 3-D Interconnect Technology Landscape
- Experimental Insights into Thermal Dissipation in TSV-Based 3-D Integrated Circuits
- Reliability Challenges Related to TSV Integration and 3-D Stacking
- Innovative Failure Analysis Techniques for 3-D Packaging Developments

Robust 3-D Stacked ICs

VOLUME 33 NUMBER 3

Contents

May/June 2016
Volume 33 Number 3

Copublished by the IEEE Council on Electronic Design Automation, the IEEE Circuits and Systems Society, the IEEE Solid-State Circuits Society, and the Test Technology Technical Council

Special Section

6 **Guest Editors' Introduction: Robust 3-D Stacked ICs**
Saqib Khursheed, Pascal Vivet, Fabian Hopsch, and Erik Jan Marinissen

8 **The 3-D Interconnect Technology Landscape**
Eric Beyne

21 **Experimental Insights Into Thermal Dissipation in TSV-Based 3-D Integrated Circuits**
Perceval Coudrain, Papa Momar Souare, Rafael Prieto, Vincent Fiori, Alexis Farcy, Laurent Le Pailleur, Jean-Philippe Colonna, Cristiano Santos, Pascal Vivet, Haykel Ben-Jamaa, Denis Dutoit, François de Crécy, Sylvain Dumas, Christian Chancel, Didier Lattard, and Severine Chéramy

37 **Reliability Challenges Related to TSV Integration and 3-D Stacking**
Kristof Croes, Joke De Messemaeker, Yunlong Li, Wei Guo, Olalla Varela Pedreira, Vladimir Cherman, Michele Stucchi, Ingrid De Wolf, and Eric Beyne

46 **Innovative Failure Analysis Techniques for 3-D Packaging Developments**
Frank Altmann and Matthias Petzold

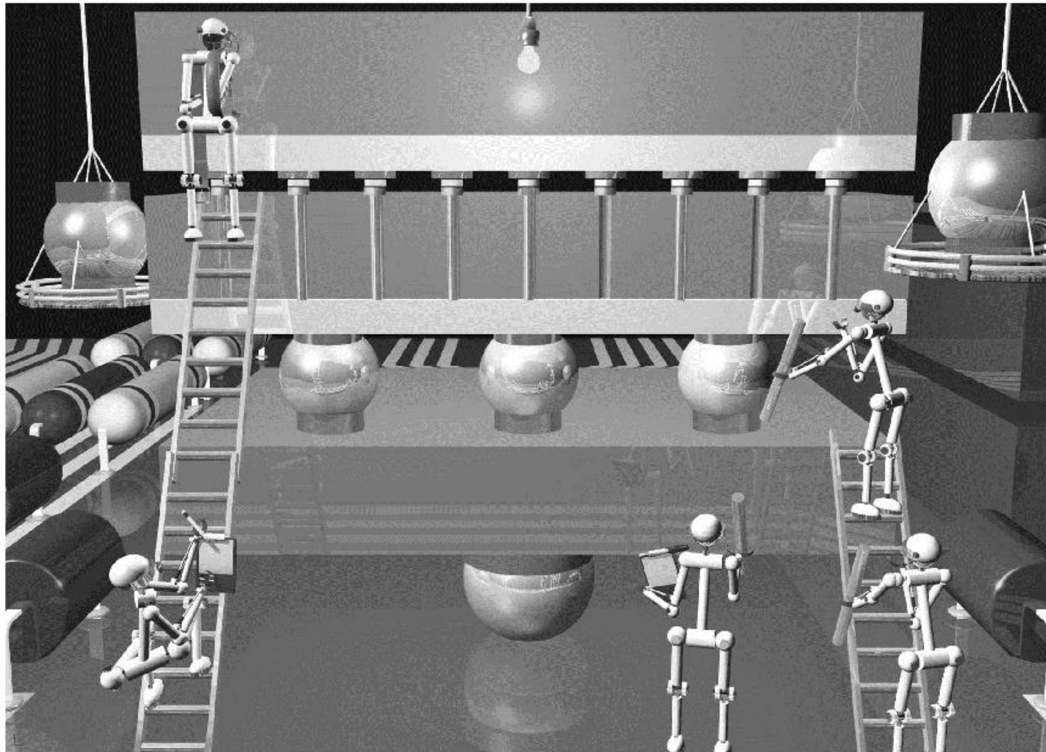
General Interest

56 **Integrated Systems in the More-Than-Moore Era: Designing Low-Cost Energy-Efficient Systems Using Heterogeneous Components**
Kaushik Roy, Byunghoo Jung, Dimitrios Peroulis, and Anand Raghunathan

66 **Designing a Cyber–Physical System for Fall Prevention by Cortico–Muscular Coupling Detection**
Daniela De Venuto, Valerio F. Annese, Michele Ruta, Eugenio Di Sciascio, and Alberto L. Sangiovanni Vincentelli

77 **Real-Time Fault Detection and Diagnosis System for Analog and Mixed-Signal Circuits of Acousto–Magnetic EAS Devices**
Qiwu Luo, Yigang He, and Yichuang Sun

ISSN 2168-2356



Cover design by Alexander Torres

DEPARTMENTS

4 From the EIC
"Robustness for 3-D Circuits—Industrial Perspectives"
Jörg Henkel

91 Tutorials
"Toward Silicon-Based Cognitive Neuromorphic ICs—A Survey"
Georgios Volanis, Angelos Antonopoulos, Yiorgos Makris, and Alkis A. Hatzopoulos

103 **"PUFs as Promising Tools for Security in Internet of Things"**
Debdeep Mukhopadhyay

116 Perspectives
"High-Level Synthesis: Status, Trends, and Future Directions"
Andres Takach

125 Interview
"Accellera's DVCon Conferences Focus on the Community of Practicing Engineers"
Gabe Moretti

133 Conference Reports
"2016 ASP-DAC"
Hidetoshi Onodera

135 Call for Special Issue Contributions
Special Issue on "Critical and Enabling Techniques for Emerging Memories"

136 **Special Issue on "Emerging Challenges and Solutions in SoC Verification"**

137 CEDA Currents

140 TTTC Newsletter

142 In Memoriam
Steven P. Levitan (1950–2016)
Mary Jane Irwin and Soha Hassoun

144 The Last Byte
"And He Built a Crooked Chip"
Scott Davidson

IEEE
Design&Test