IEEE TRANSACTIONS ON

CIRCUITS AND SYSTEMS

II: EXPRESS BRIEFS

A PUBLICATION OF THE IEEE CIRCUITS AND SYSTEMS SOCIETY

WWW.IEEE-CAS.ORG

MAY 2016 VOLUME 63 NUMBER 5 ITCSFK (ISSN 1549-7747)

Analog and Mixed Mode Circuits and Systems

A 0.0054-mm^2 Frequency-to-Current Conversion-Based Fractional Frequency Synthesizer in 32 nm Utilizing Deep Trench Capacitor . . . . . *S. Kundu and C. H. Kim* 413

CMOS Transimpedance Amplifier for Gigabit-per-Second Optical Wireless Communications . . . . . *R. Y. Chen and Z.-Y. Yang* 418

A Novel Window Function for Memristor Model With Application in Programming Analog Circuits . . . . . *J. Zha, H. Huang, and Y. Liu* 423

An Accurate Bandgap-Based Power-on-Detector in 14-nm CMOS Technology. . . . . *J. Shor and D. Zilberman* 428

Design Techniques for Linearity in Time-Based $\Sigma\Delta$ Analog-to-Digital Converter. . . . . *M. Amin and B. Leung* 433

Charge-Withheld Converter-Reshuffling: A Countermeasure Against Power Analysis Attacks . . . . . *W. Yu and S. Köse* 438

A 12.5 mW, 11.1 nV/$\sqrt{\text{Hz}}$, -115 dB THD, < 1 μs Settling, 18 bit SAR ADC Driver in 0.6 μm CMOS . . . . . *K. S. Rakshitdatta, Y. Mitikiri, and N. Krishnapura* 443

A 330-μW 400-MHz BPSK Transmitter in 0.18-μm CMOS for Biomedical Applications . . . . . *Y.-L. Tsai, C.-Y. Lin, B.-C. Wang, and T.-H. Lin* 448

A Self-Calibrated Bang–Bang Phase Detector for Low-Offset Time Signal Processing . . . . . *J. Prinzie, M. Steyaert, and P. Leroux* 453

Low-Power ASK Detector for Low Modulation Indexes and Rail-to-Rail Input Range . . . . . *V. Fiore, E. Ragonese, and G. Palmisano* 458

Digital Circuits and Systems and VLSI

Digital Multiplierless Realization of Two-Coupled Biological Hindmarsh–Rose Neuron Model . . . . . *M. Hayati, M. Nouri, D. Abbott, and S. Haghiri* 463

Macromodels for Static Virtual Ground Voltage Estimation in Power-Gated Circuits . . . . . *L. Garg and V. Sahula* 468

An FPGA Implementation for Solving the Large Single-Source-Shortest-Path Problem . . . . . *G. Lei, Y. Dou, R. Li, and F. Xia* 473

High-Speed Hardware Implementation of Fixed and Runtime Variable Window Length 1-D Median Filters . . . . . *E. Nikahd, P. Behnam, and R. Sameni* 478

(Contents Continued on Back Cover)

(Contents Continued from Front Cover)

Signal Processing

Low-Complexity First-Two-Minimum-Values Generator for Bit-Serial LDPC Decoding . . . . . *J. H. Lee and M. H. Sunwoo* 483

Single-Exposure HDR Technique Based on Tunable Balance Between Local and Global Adaptation . . . . . *J. Fernández-Berni, R. Carmona-Galán, and Á. Rodríguez-Vázquez* 488

Combined-Step-Size Affine Projection Sign Algorithm for Robust Adaptive Filtering in Impulsive Interference Environments . . . . . *F. Huang, J. Zhang, and S. Zhang* 493

Control Theory and Systems

Tradeoffs Between Transmission Intervals and Delays for Decentralized Networked Control Systems Based on a Gain Assignment Approach. . . . . *K.-Z. Liu, R. Wang, and G.-P. Liu* 498

Circuits and Systems for Communications

A UWB-Based Sensor-to-Time Transmitter for RF-Powered Sensing Applications . . . . . *J. Mao, Z. Zou, and L.-R. Zheng* 503

Power Systems and Electronic Circuits

DTMOS-Based Pulse Transformer Boost Converter With Complementary Charge Pump for Multisource Energy Harvesting. . . . . *Y.-K. Teh and P. K. T. Mok* 508