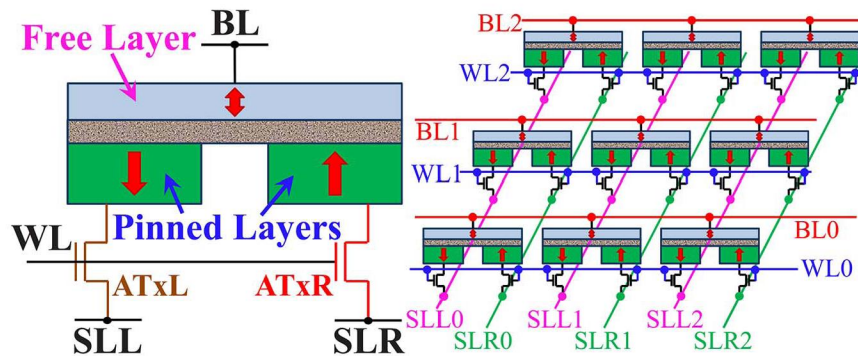


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Proposed CPSTT-MRAM structure with organization of memory array. From the paper,
“Non-Volatile Complementary Polarizer Spin-Transfer Torque On-Chip Caches:
A Device/Circuit/Systems Perspective,” by X. Fong *et al.*, on p. 3400611.

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