

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS

A JOINT PUBLICATION OF THE IEEE CIRCUITS AND SYSTEMS SOCIETY 
THE IEEE COMPUTER SOCIETY 
THE IEEE SOLID-STATE CIRCUITS SOCIETY 

JANUARY 2016

VOLUME 24

NUMBER 1

ITCOB4

(ISSN 1063-8210)

REGULAR PAPERS

Power Delivery, Harvesting, and Distribution

A System-Level Cosynthesis Framework for Power Delivery and On-Chip Data Networks in Application-Specific 3-D ICs	<i>N. Kapadia and S. Pasricha</i>	3
A Fast-Transient Wide-Voltage-Range Digital-Controlled Buck Converter With Cycle-Controlled DPWM	<i>W.-C. Chen, C.-C. Chen, C.-Y. Yao, and R.-J. Yang</i>	17
A Thermal Energy Harvesting Power Supply With an Internal Startup Circuit for Pacemakers	<i>M. Ashraf and N. Masoumi</i>	26
Test Pattern Modification for Average IR-Drop Reduction	<i>W.-S. Ding, H.-Y. Hsieh, C.-Y. Han, J. C.-M. Li, and X. Wen</i>	38

Digital Circuits and Systems

Speculative Lookahead for Energy-Efficient Microprocessors	<i>T.-J. Lin and T.-Y. Shyu</i>	50
Assessing Trends in Performance per Watt for Signal Processing Applications	<i>B. Degnan, B. Marr, and J. Hasler</i>	58
A Mixed-Decimation MDF Architecture for Radix-2 ^k Parallel FFT	<i>J. Wang, C. Xiong, K. Zhang, and J. Wei</i>	67
Evaluation and Tradeoffs for Out-of-Order Execution on Reconfigurable Heterogeneous MPSoC	<i>Q. Guo, X. Li, C. Wang, and X. Zhou</i>	79
Enhanced Wear-Rate Leveling for PRAM Lifetime Improvement Considering Process Variation	<i>Y. Han, J. Dong, K. Weng, Y. Wang, and X. Li</i>	92

Nonvolatile Circuits and Systems

EqualWrites: Reducing Intra-set Write Variations for Enhancing Lifetime of Non-Volatile Caches	<i>S. Mittal and J. S. Vetter</i>	103
LBA Scrambler: A NAND Flash Aware Data Management Scheme for High-Performance Solid-State Drives	<i>C. Sun, A. Soga, C. Matsui, A. Arakawa, and K. Takeuchi</i>	115
Reducing Switching Latency and Energy in STT-MRAM Caches With Field-Assisted Writing	<i>R. Patel, X. Guo, Q. Guo, E. Ipek, and E. G. Friedman</i>	129

(Contents Continued on Page 1)



<i>Field-Programmable Gate Arrays</i>	
High-Density and High-Reliability Nonvolatile Field-Programmable Gate Array With Stacked 1D2R RRAM Array	K. Huang, R. Zhao, W. He, and Y. Lian 139
A High-Speed FPGA Implementation of an RSD-Based ECC Processor	H. Marzouqi, M. Al-Qutayri, K. Salah, D. Schinianakis, and T. Stouraitis 151
Power Analysis of Embedded NoCs on FPGAs and Comparison With Custom Buses	M. S. Abdelfattah and V. Betz 165
An FPGA Architecture and CAD Flow Supporting Dynamically Controlled Power Gating	A. A. M. Bsoul, S. J. E. Wilton, K. H. Tsoi, and W. Luk 178
<i>Circuits and Systems in Emerging Technologies</i>	
PROCEED: A Pareto Optimization-Based Circuit-Level Evaluator for Emerging Devices	S. Wang, A. Pan, C. O. Chui, and P. Gupta 192
Alternative Architectures Toward Reliable Memristive Crossbar Memories	I. Vourkas, D. Stathis, G. Ch. Sirakoulis, and S. Hamdioui 206
A Low-Power Robust Easily Cascaded PentaMTJ-Based Combinational and Sequential Circuits	M. K. Gupta and M. Hasan 218
<i>Analog Techniques</i>	
Using the Gate–Bulk Interaction and a Fundamental Current Injection to Attenuate IM3 and IM2 Currents in RF Transconductors	M. Asghari and M. Yavari 223
Placement-Based Nonlinearity Reduction Technique for Differential Current-Steering DAC	N. Pal, P. Nandi, R. Biswas, and A. G. Katakwar 233
A 5-/20-MHz BW Reconfigurable Quadrature Bandpass CT $\Delta\Sigma$ ADC With Anti-Pole-Splitting Opamp and Digital I/Q Calibration	Y. Xu, Z. Zhang, B. Chi, N. Qi, H. Cai, and Z. Wang 243
A Fully Digital Front-End Architecture for ECG Acquisition System With 0.5 V Supply	M. Zare and M. Maymandi-Nejad 256
<i>Specialized Processing and Security</i>	
Code Compression for Embedded Systems Using Separated Dictionaries	W. J. Wang and C. H. Lin 266
Sequence-Aware Watermark Design for Soft IP Embedded Processors	J. Kufel, P. R. Wilson, S. Hill, B. M. Al-Hashimi, and P. N. Whatmough 276
A Novel Thyristor-Based Silicon Physical Unclonable Function	C. Bai, X. Zou, and K. Dai 290
<i>Verification and Testing</i>	
Source Code Error Detection in High-Level Synthesis Functional Verification	B. Carrion Schafer 301
Efficient Selection of Trace and Scan Signals for Post-Silicon Debug	K. Rahmani, S. Proch, and P. Mishra 313
TRANSACTIONS BRIEFS	
Tunable Multiprocess Mapping on Coarse-Grain Reconfigurable Architectures With Dynamic Frequency Control	B. Carrion Schafer 324
TCAD-Assisted Capacitance Extraction of FinFET SRAM and Logic Arrays	D. Bhattacharya and N. K. Jha 329
Exploiting Process Variation for Write Performance Improvement on NAND Flash Memory Storage Systems	L. Shi, Y. Di, M. Zhao, C. J. Xue, K. Wu, and E. H.-M. Sha 334
Network-on-Chip for Turbo Decoders	Q. Yang, X. Zhou, G. E. Sobelman, and X. Li 338
ContextPreRF: Enhancing the Performance and Energy of GPUs With Nonuniform Register Access	M. Moeng, H. Xu, R. Melhem, and A. K. Jones 343
Transimpedance Limit Exploration and Inductor-Less Bandwidth Extension for Designing Wideband Amplifiers	O. T.-C. Chen, C.-T. Chan, and R. R.-B. Sheen 348
A Cellular Network Architecture With Polynomial Weight Functions	J. Müller, J. Müller, R. Braunschweig, and R. Tetzlaff 353
Single-Supply 3T Gain-Cell for Low-Voltage Low-Power Applications	R. Güterman, A. Teman, P. Meinerzhagen, L. Atias, A. Burg, and A. Fish 358
All-Digital Duty-Cycle Corrector With a Wide Duty Correction Range for DRAM Applications	C.-H. Jeong, A. Abdullah, Y.-J. Min, I.-C. Hwang, and S.-W. Kim 363
Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic	K. Tsoumanis, S. Xydis, G. Zervakis, and K. Pekmestzi 368

A Single-Ended With Dynamic Feedback Control 8T Subthreshold SRAM Cell	<i>C. B. Kushwah and S. K. Vishvakarma</i>	373
Effectiveness of Low-Voltage Testing to Detect Interconnect Open Defects Under Process Variations	<i>J. Moreno, M. Renovell, and V. Champac</i>	378
A Dynamically Reconfigurable Multi-ASIP Architecture for Multistandard and Multimode Turbo Decoding	<i>V. Lapotre, P. Murugappa, G. Gogniat, A. Baghdadi, M. Hübner, and J.-P. Diguët</i>	383
Defect Diagnosis via Segment Delay Learning	<i>J. Chung and W. Kang</i>	388
In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers	<i>B. Ghoshal, K. Manna, S. Chattopadhyay, and I. Sengupta</i>	393
Energy and Area Efficient Three-Input XOR/XNORS With Systematic Cell Design Methodology	<i>T. Nikoubin, M. Grailoo, and C. Li</i>	398
Polymorphic Configuration Architecture for CGRAs	<i>S. M. A. H. Jafri, M. A. Tajammul, A. Hemani, K. Paul, J. Plosila, P. Ellervee, and H. Tenunnen</i>	403
A 0.52/1 V Fast Lock-in ADPLL for Supporting Dynamic Voltage and Frequency Scaling	<i>C.-C. Chung, W.-S. Su, and C.-K. Lo</i>	408
