

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS

A JOINT PUBLICATION OF THE IEEE CIRCUITS AND SYSTEMS SOCIETY
THE IEEE COMPUTER SOCIETY
THE IEEE SOLID-STATE CIRCUITS SOCIETY



MARCH 2016

VOLUME 24

NUMBER 3

ITCOB4

(ISSN 1063-8210)

REGULAR PAPERS

Computational and Arithmetic Units

Symbiote Coprocessor Unit—A Streaming Coprocessor for Data Stream Acceleration	<i>P. S. Vaidya, J. J. Lee, V. S. Pai, M. Lee, and S. Hur</i>	813
A Novel Quantum-Dot Cellular Automata X -bit \times 32-bit SRAM	<i>M. Kianpour and R. Sabbaghi-Nadooshan</i>	827
Hardware Accelerator for Probabilistic Inference in 65-nm CMOS	<i>O. U. Khan and D. D. Wentzloff</i>	837
Input-Based Dynamic Reconfiguration of Approximate Arithmetic Units for Video Encoding	<i>A. Raha, H. Jayakumar, and V. Raghunathan</i>	846

Energy-Efficient Resilient Digital Techniques

VANUCA: Enabling Near-Threshold Voltage Operation in Large-Capacity Cache	<i>Y. Wang, Y. Han, H. Li, and X. Li</i>	858
Write Buffer-Oriented Energy Reduction in the L1 Data Cache for Embedded Systems	<i>J. Lee and S. Kim</i>	871
Designing Tunable Subthreshold Logic Circuits Using Adaptive Feedback Equalization	<i>M. Zangeneh and A. Joshi</i>	884
Error Resilient and Energy Efficient MRF Message-Passing-Based Stereo Matching	<i>E. P. Kim, J. Choi, N. R. Shanbhag, and R. A. Rutenbar</i>	897
Process Variation Delay and Congestion Aware Routing Algorithm for Asynchronous NoC Design	<i>R. Ezz-Eldin, M. A. El-Moursy, and H. F. A. Hamed</i>	909
DFSB-Based Thermal Management Scheme for 3-D NoC-Bus Architectures	<i>J. Zheng, N. Wu, L. Zhou, Y. Ye, and K. Sun</i>	920
Low-Cost Multiple Bit Upset Correction in SRAM-Based FPGA Configuration Frames	<i>M. Ebrahimi, P. M. B. Rao, R. Seyyedi, and M. B. Tahoori</i>	932

Memory Arrays

Adaptive Write and Shift Current Modulation for Process Variation Tolerance in Domain Wall Caches	<i>S. Motaman and S. Ghosh</i>	944
Sequoia: A High-Endurance NVM-Based Cache Architecture	<i>M. R. Jokar, M. Arjomand, and H. Sarbazi-Azad</i>	954
A Universal Hardware-Driven PVT and Layout-Aware Predictive Failure Analytics for SRAM	<i>R. Joshi, S. Saroop, R. Kanj, Y. Liu, W. Wang, C. Radens, Y. Tan, and K. Yogendra</i>	968

(Contents Continued on Back Cover)



(Contents Continued from Front Cover)

An Information Theory Perspective for the Binary STT-MRAM Cell Operation Channel	<i>J. Yang, B. Geller, M. Li, and T. Zhang</i>	979
Embedding Read-Only Memory in Spin-Transfer Torque MRAM-Based On-Chip Caches	<i>X. Fong, R. Venkatesan, D. Lee, A. Raghunathan, and K. Roy</i>	992
Modeling and Optimization of Memristor and STT-RAM-Based Memory for Low-Power Applications	<i>Y. Halawani, B. Mohammad, D. Homouz, M. Al-Qutayri, and H. Saleh</i>	1003
<i>Circuits for Analog, Communications, and Security</i>		
All-Digital 90° Phase-Shift DLL With Dithering Jitter Suppression Scheme	<i>D.-H. Jung, K. Ryu, J.-H. Park, and S.-O. Jung</i>	1015
An All-Digital Approach to Supply Noise Cancellation in Digital Phase-Locked Loop	<i>W. Namgoong</i>	1025
Enhancing Model Order Reduction for Nonlinear Analog Circuit Simulation	<i>H. Aridhi, M. H. Zaki, and S. Tahar</i>	1036
Dual-Calibration Technique for Improving Static Linearity of Thermometer DACs for I/O	<i>I. Mukhopadhyay, M. Y. Mukadam, R. Narayanan, F. O'Mahony, and A. B. Apsel</i>	1050
DScanPUF: A Delay-Based Physical Unclonable Function Built Into Scan Chain	<i>Y. Zheng, F. Zhang, and S. Bhunia</i>	1059
Toward Solving Multichannel RF-SoC Integration Issues Through Digital Fractional Division	<i>S. A. R. Ahmadi Mehr, M. Tohidian, and R. B. Staszewski</i>	1071
A Low-Power and Highly Linear 14-bit Parallel Sampling TDC With Power Gating and DEM in 65-nm CMOS	<i>S. Liu and Y. Zheng</i>	1083
An Add-On Type Real-Time Jitter Tolerance Enhancer for Digital Communication Receivers	<i>S. Hwang, J. Song, S.-G. Bae, Y. Lee, and C. Kim</i>	1092
A Two-Step Analog Accumulator for CMOS TDI Image Sensor With Temporal Undersampling Exposure Method	<i>Y. Xia, K. Nie, J. Xu, and S. Yao</i>	1104
Dual Use of Power Lines for Design-for-Testability—A CMOS Receiver Design	<i>J. M. Salem and D. S. Ha</i>	1118
<i>Algorithms</i>		
GenFin: Genetic Algorithm-Based Multiobjective Statistical Logic Circuit Optimization Using Incremental Statistical Analysis	<i>A. Tang and N. K. Jha</i>	1126
GPU-Accelerated Parallel Sparse LU Factorization Method for Fast Circuit Analysis	<i>K. He, S. X.-D. Tan, H. Wang, and G. Shi</i>	1140
A Generally Applicable Calibration Algorithm for Digitally Reconfigurable Self-Healing RFICs	<i>E. J. Wyers, M. A. Morton, T. C. L. G. Sollner, C. T. Kelley, and P. D. Franzon</i>	1151
TRANSACTIONS BRIEFS		
Ultralow-Energy Variation-Aware Design: Adder Architecture Study	<i>H. Dorosti, A. Teymouri, S. M. Fakhraie, and M. E. Salehi</i>	1165
High-Performance Deadlock-Free ID Assignment for Advanced Interconnect Protocols	<i>H.-M. Chou, Y.-C. Chen, K.-H. Yang, J. Tsao, S.-C. Chang, W.-B. Jone, and T.-F. Chen</i>	1169
Low-Power Variation-Tolerant Nonvolatile Lookup Table Design	<i>X. Xue, J. Yang, Y. Lin, R. Huang, Q. Zou, and J. Wu</i>	1174
Design-Time Reliability Enhancement Using Hotspot Identification for RF Circuits	<i>D. Chang, J. N. Kitchen, B. Bakaloglu, S. Kiaei, and S. Ozev</i>	1179
A 0.4-mW, 4.7-ps Resolution Single-Loop $\Delta\Sigma$ TDC Using a Half-Delay Time Integrator	<i>C.-K. Kwon, H. Kim, J. Park, and S.-W. Kim</i>	1184
Skew Minimization With Low Power for Wide-Voltage-Range Multipower-Mode Designs	<i>C.-H. Chou, H.-H. Yeh, S.-H. Huang, Y.-T. Nieh, S.-C. Chang, and Y.-T. Chang</i>	1189
A Practical Logic Obfuscation Technique for Hardware Security	<i>J. Zhang</i>	1193
Diagnostic Fail Data Minimization Using an N -Cover Algorithm	<i>S. Bodhe, M. E. Amyeen, I. Pomeranz, and S. Venkataraman</i>	1198
Histogram-Based Ratio Mismatch Calibration for Bridge-DAC in 12-bit 120 MS/s SAR ADC	<i>Y. Zhu, C.-H. Chan, S.-S. Wong, U Seng-Pan, and R. P. Martins</i>	1203
Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation	<i>A. Kaivani and S. Ko</i>	1208
COMMENTS AND CORRECTIONS		
Corrections to “GPU-Accelerated Parallel Sparse LU Factorization Method for Fast Circuit Analysis”	<i>K. He and S. Tan</i>	1212
